

What is claimed is:

1 1. A method of eliminating parasitic bipolar transistor
2 action in a Silicon on Insulator (SOI) Metal Oxide
3 Semiconductor (MOS) device, the method comprising:
4 Controlling the conduction of an active discharging
5 device, said active discharging device being coupled to said
6 SOI device, whereby the parasitic bipolar transistor is
7 deactivated.

1 2. The method of claim 1 further comprising:
2 providing a first signal to a first node of said SOI
3 device;
4 providing a second signal to an input of said SOI
5 device; and
6 activating the conduction of said active discharging
7 device according to the state of said first and second
8 signals.

1 3. The method of claim 2 wherein the first signal is a
2 clock signal.

1 4. The method of claim 3 wherein said first node is
2 charged high whenever said clock signal is active low.

1 7. A method of eliminating parasitic bipolar transistor
2 action in a Silicon on Insulator (SOI) Metal Oxide
3 Semiconductor (MOS) dynamic logic circuit having an input an
4 output, a clock, a plurality of stacked SOI Metal Oxide
5 Semiconductor (MOS) transistors interconnected to perform a
6 predetermined logic function defining a common node and an
7 intermediate node, said plurality of stacked SOI MOS
8 transistors being controlled by a respective plurality of
9 inputs, said common node being coupled to a pre-charging
10 device and said intermediate node being in a path between
11 said common node and a discharge potential, said path
12 defined by said plurality of stacked SOI MOS transistors,
13 said intermediate node being coupled to said common node by
14 at least a first of said plurality of stacked SOI MOS
15 transistors, and said intermediate node being coupled to
16 said discharge potential by at least a second of said
17 plurality of stacked SOI MOS transistors, and an active
18 discharging transistor controlled by at least one of said
19 plurality of inputs, said active discharging transistor
20 defining a discharge path between said intermediate node and
21 said discharge potential, the method comprising:

22 controlling the conduction of said active discharging
23 transistor during a pre-charge cycle; and

24 actively discharging said intermediate nodes of the SOI
25 stacked transistors, whereby the parasitic bipolar
26 transistors are deactivated and the charge at said common

27 node is maintained at a predetermined level.

1 8. The method according to claim 7, wherein pre-charging
2 occurs during a low state of said clock.

1 9. The method according to claim 7, wherein pre-charging
2 occurs during a high state of said clock.

1 10. The method according to claim 7, wherein during the
2 pre-charging all said inputs are set to a predetermined
3 logic state.

1 11. The method according to claim 10, wherein said logic
2 state is low.

1 12. The method according to claim 10, wherein said logic
2 state is high.

1 13. The method according to claim 7, wherein the step of
2 actively discharging said intermediate nodes prevents the
3 body voltages of said stacked SOI transistors from reaching
4 a voltage stage sufficient to activate the parasitic bipolar
5 transistors of said stacked SOI transistors.

1 14. The method according to claim 7, wherein said stacked
2 transistors are N-Field Effect Transistors (NFET) and said
3 active discharging transistors are P-Field Effect
4 Transistors (PFET).

1 15. The method according to claim 7, wherein said stacked
2 transistors are P-Field Effect Transistors (PFET) and said
3 active precharging transistors are N-Field Effect
4 Transistors (NFET).

1 16. The method according to claim 7, wherein said pre-
2 charging device comprises transistors coupled to said
3 stacked transistors.